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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE (211.004-US)

In re Application of: FERRANT ET AL.

U.S. Application Serial No: 10/840,009

U.S. Filing Date: MAY 6, 2004

Title: SEMICONDUCTOR MEMORY DEVICE AND

METHOD OF OPERATING SAME

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Group Art Unit: 2818

Examiner:

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to the Commissioner for Patents, P.O. Bcx 1450, Alexandria, VA 22313-1450 on Alexandria, VA

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SECOND INFORMATION DISCLOSURE STATEMENT

Dear Sir.

Submitted herewith are seven (7) sheets of modified Form PTO-1449. A copy of each document identified on the Form PTO-1449 is also submitted.

It is respectfully requested that the Examiner make his/her consideration of these documents formally of record with the initial Office Action.

Respectfully submitted,

Date: August 11, 2004

Neil A. Steinberg Reg. No. 34,735

650-968-8079



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		Double-Gate C	RAM Cell", Kuo et al., IEEE Ele		etters, Vo	I. 23, I	No.
	"A Capacitorless 2002, pp.843-946	Double-Gate D	RAM Cell for High Density Appli	cations", Kuo	et al., IEE	E IED	М,
	"The Multi-Stable 1988 SOS/SOI Te	Behaviour of S echnology Wor	GOI-NMOS Transistors at Low Te kshop (Sea Palms Resort, St. Si	emperatures", imons Island,	Tack et al GA, Oct. 1	., Proc 988).	c. p.78
	"The Multistable C Tack et al., IEEE	Charge-Control Transactions o	led Memory Effect in SOI MOS 1 n Electron Devices, Vol. 37, No.	ransistors at 5, May 1990,	Low Temp pp.1373-1	eratur 1382	es",
	"Mechanisums of DRAMs", Villaret	Transactions o Charge Modul at al., Proceed	led Memory Effect in SOI MOS In Electron Devices, Vol. 37, No. ation in the Floating Body of Triplings of the INFOS 2003, Instual Conference, June 18-20, 2015	5, May 1990, le-Well nMOS	pp.1373-1 FET Cape on	382 citor-	less
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	"Memory Design to State Circuits, Vol	Jsing a One-Tr J. 37, No. 11, N	ansisto ovemb	or Gain Cell on SOI", Oh: er 2002, pp.1510-1522	sawa et al., IEB	EE Journa	l of Sc	olid-
	"Opposite Side Flo	pating Gate SC) FLAS	SH Memory Cell", Lin et	al., IEEE, Marc	h 2000, pp	p.12-1	15
				Using a Phase-Shift Litt 42, No. 7, July 1995, pp		nanaka et	al., IE	EEE
	"Soft-Error Charac Transactions on E	teristics in Bip lectron Device	olar Me s, Vol.	emory Cells with Small C 38, No. 11, November 1	ritical Charge" 991, pp.2465-2	, Idei et al. 2471	, IEEI	E
	"An SOI 4 Transis 2003, pp.401-404	tors Self-Refre	sh Ultra	-Low-Voltage Memory (Cell", Thomas	et al. IEEE	E, Mar	rch
	*Design of a SOI Microelectronics (I	Jemory Cell", 5 MIEL '97), Vol.	Stanoje 1, NIS,	vic et al., IEEE Proc. 21 Yugoslavis, 14-17 Sept	st International tember 1997, p	Conference p.297-300	e on	
	"Effects of Floating Chan et al., IEEE	Body on Doul Electron Device	ble Pol	ysilicon Partially Depleters, Vol. 24, No. 2, Februa	od SOI Nonvola ary 2003, pp.79	itile Memo 5-77	ry Ce	ir.
	"MOSFET Design	Simplifies DRA	\М", Р.	Fazan, EE Times, May	14, 2002 (3 pa	ges)	,	
	"One of Application International Confe pp.455-458	n of SOI Memo erence on Micr	ry Cell oelectr	– Memory Array", Lonca onics (MIEL 2000), Vol.	ar et al., IEEE F 2, NIŠ, Serbla,	² roc, 22 nd 14- 7 Ma	y 200	0,
	"A SOI Current Me IEEE International	mory for Analo SOI Conference	g Sign ce, Oct	al Processing at High Te . 1999, pp.18-19	emperature", P	ortmann e	t al., 1	1999
	"Chip Level Reliab International SOI C	ility on SOI Em Conference, Oc	bedde t. 1998	d Memory", Kirn et al., P 3, pp.135-139	roceedings 19	98 IE:EE		
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i	"Analysis of Floati	ing-Body-Induce	ed Leaka	ge Current in 0.15µ Conference, Oct. 19	m SOI DRAM",	Terauchi e	et al.,	
	Fabricated on SO	l Wafers", Chi e	ating-Bo	dy for High Density	ow Voltage Fi	sh EEPRO	OM ence.	Oct.
	"Programming and Fabricated on SO 1995, pp.129-130	l Wafers", Chi e	ating-Bo t al., Pro		ow Voltage Fi	sh EEPRO	OM ence,	Oct.
	Fabricated on SO 1995, pp.129-130 "Measurement of	I Wafers", Chi e	t al., Pro	dy for High Density	ow Voltage Flands International S	ash EEPRO OI Confer	ence,	Oct.
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 OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)
"The Multistable Charge Controlled Memory Effect in SOI Transistors at Low Temperatures". Tack et al., IEEE Workshop on Low Temperature Electronics, 7-8 Aug. 1989, University of Vermont, Burlington, pp.137-141
"High-Endurance Ultra-Thin Tunnel Oxide in MONOS Device Structure for Dynamic Memory Application", Wann et al., IEEE Electron Device Letters, Vol. 16, No. 11, November 1995, pp.491-493
"Hot-Carrier Effects in Thin-Film Fully Depleted SOI MOSFET's", Ma et al., IEEE Electron Device Letters, Vol. 15, No. 6, June 1994, pp.218-220
"Design Analysis of Thin-Body Sliiclde Source/Drain Devices", 2001 IEEE International SOI Conference, October 2001, pp.21-22
"SOI MOSFET on Low Cost SPIMOX Substrate", lyer et al., IEEE IEDM, Septembe 1998, pp.1001-1004
"Simulation of Floating Body Effect In SOI Circuits Using BSIM3SOI", Tu et al., Proceedings of Technical Papers (IEEE Cat No. 97 TH 8303), pp.339-342
"High-Field Transport of Inversion-Layer Electrons and Holes Including Velocity Overshoot", Assaderaghi et al., IEEE Transactions on Electron Devices, Vol. 44, No. 4, April 1997, pp.684-671
"Dynamic Threshold-Voltage MOSFET (DTMOS) for Ultra-Low Voltage VLSI", Assaderaghi et al., IEEE Transactions on Electron Devices, Vol. 44, No. 3, March 1997, pp.414-422
"Hot-Carrier-Induced Degradation in Ultra-Thin-Film Fully-Depleted SOI MOSFETs", Yu et al., Solid-State Electronics, Vol. 39, No. 12, 1996, pp.1791-1794
"Hot-Carrier Effect in Ultra-Thin-Film (UTF) Fully-Depleted SOI MOSFET's, Yu et al., 54th Annual Device Research Conference Digest (Cat. No. 96 TH 8193), pp.22-23

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	"SOI MOSFET Des Films", Chan et al.	sign for All-Dime , IEEE IEDM, 1	ension 995, p	ial Scaling with Short Cha p.631-634	annel, Narrov	/Width an	d Uittr	a-thin
	"A Novel Silicon-O 1994 IEEE Sympo	n-Insulator (SO sium on Low Po	i) MOS	SFET for Ultra Low Voltac Electronics, pp.58-59	ge Operation'	, Assader	aghi e	et al.,
	"Interface Characteral., Proceedings 19	erization of Full 194 IEEE Intern	ly-Depl nationa	eted SOI MOSFET by a 5	Subthreshold 994, pp.63-6		đ", Yu	ı et
		ouble-Gate DR		ell Design for High Densit			al., (E	EE
		•	ngeei	(DTMOS) for Ultra-Low	Voltage One	rotion [®] Ac		
	et al., IEEE Electro	n Device Letter	rs, Vol.	. 15, No. 12, December 1	994, pp.510-	512	saden	agnı
	"Dynamic Threshol al., 1994 EEE, IED	d-Voltage MOS M 94, pp.809-8	SFET (1 312	DTMOS) for Ultra-Low Vo	oltage Operat	ion", Assa	derag	ihi et
	"A Capacitorless D	RAM Cell on S	OI Sub	ostrate", Wann et al., IEE	E IEDM 1993	, pp.635-6	38	
l l	"Studying the Impa Using BSIMPD", St Design (ISQED '02	ı et al., IEEE Pi	roceed	on Dynamic Behaviors of lings of the International i)	Partially-Dep Symposium o	pleted SOI on Quality	CMO Electr	S onic
	MOS Structures by	the Charge-Pu	ımping	iiO₂ Interfaces in Thick- a Technique", Wouters et nber 1989, pp.1746-1750	al IEEE Tra	Silicon-on neactions	-Insul on	ator
	"An Analytical Mode Electronics Vol. 33,	el for the Misis No. 3, 1990, p	Structi p.357-	ure in SOI MOS Devices" 364	, Tack et al.,	Solid State	≥	
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	"A Simple 1-Trans Fazan et al., IEEE	istor Capacitor 2002 Custom	r-Less Integra	Memory Cell for High Pe ated Circults Conference	erformance Em e, June 2002, p	bedded DI p.99-102	RAMs	7.
	"High-Endurance Application", Wan 493	Ultra-Thin Tuni n et al., IEEE E	nel Oxi	de in MONOS Device St n Device Letters, Vol. 16	ructure for Dyr , No. 11, Nove	amic Merr mber 1995	iory i, pp.4	191-
	"Capacitor-Less 1- 2002, pp.10-13	-Transistor DR	AM", F	azan et al., 2002 IEEE ii	nternational SC	Ol Confere	nce, (Oct.
	"SOI (Silicon-on-In Phys. Vol. 33 (199	nsulator) for Hig 4) pp.365-369,	gh Spe , Part 1	ed Ultra Large Scale Into No. 1B, January 1994	egration", C, H	u, Jpn. J. A	\ppl.	
	"Source-Bias Depo Memory Cell Trans 3B, March 1998	endent Charge sistors", Sim et	Accun al., Jp	nulation in P+ -Poly Gate n. J. Appl. Phys. Vol. 37	SOI Dynamic (1998) pp.126	Random / 0-1263, Pa	Acces art 1,	s No.
	"Suppression of Pa by Ar-lon Implanta Devices, Vol. 45, N	tion into Sourc	e/Drain	in Ultra-Thìn-Film Fully- Regions", Ohno et al., 071-1076	Depleted CMC	S/SIMOX lons on Ele	Devic	es
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	"Fully Isolated Lat	eral Bipolar-Mi	O\$ Tra	nsistors Fabricated in Zo vice Letters, Vol. EDL-4,	ne-Melting-Re				
		tor Bipolar Tra		s", Rodder et al., IEEE E					
	"Characteristics a Polycrystalline Sil February 1985, pp	icon", Malhi et	ensiona al., IEE	I Integration of MOSFET E Transactions on Elect	's in Small-Gr ron Devices, \	ain LF'CVD /ol. E:D-32) , No. 2,		
	"Triple-Wel nMOS Density Applicatio Workshop, June 8	ns", Villaret et	al., Hai	Capecitor-Less DRAM Condout at Proceedings of in (2 pages)	ell for Nanosc 2003 Silicon N	ale Low-Co Nanoelectro	et & High onics		
	"Mechanisms of C DRAMs", Villaret e Spain (2 pages)	harge Modulat et al., Handout	tion in t	he Ficating Body of Tripl eedings of INFOS 2003,	e-Weil NMOS June 18-20,	FET Capa 2003, Baro	citor-less elona,		
				r, M. Yamawaki, Procee Technology, 1998, Vol.		ymposium	on		
	"3-Dimensional Si IEIC Technical Re Vol. 97, No. 557 (\$	port, institute d	of Elect	urrent in Partially Deplet ronics, Information and C 27-34	ed SOI MOSF Communicatio	ETs", iked n Engineer	a et al., s, 1998,		
	"DRAM Design Us Electron Devices,	ing the Taper- Vol. ED-29, No	Isolateo	l Dynamic RAM Cell, Lei ril 1982, pp.707-714	iss et al.", IEE	E Transac	tions on		
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE (211.004-US)

Filed: May 6, 2004

APPLICANT: Ferrant et al.

SER!AL NO.: 10/840,009

TITLE: Semiconductor Memory Device and Method of Operating Same

RECEIPT OF THE FOLLOWING PAPERS IS ACKNOWLEDGED

1. Second Information Disclosure Statement (1 page + Modified Form-PTO-1449 (7 pages) + Retendes cited therein)

DATE: August 11, 2004

[Check No. N/A]

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE (211.004-US)

In re Application of: FERRANT ET AL.

U.S. Application Serial No: 10/840,009

U.S. Filing Date: MAY 6, 2004

Title: SEMICONDUCTOR MEMORY DEVICE AND

METHOD OF OPERATING SAME

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Group Art Unit: 2818

Examiner:

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on Amunity, 2004

Michila Ster

(person signing this certificate)

Signature



FOURTH INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Submitted herewith are five (5) sheets of modified Form PTO-1449. A copy of each document identified on the Form PTO-1449 is also submitted.

It is respectfully requested that the Examiner make his/her consideration of these documents formally of record with the initial Office Action.

Respectfully submitted.

Date: August 12, 2004

Neil A. Steinberg

Reg. No. 34,735 650-968-8079

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	EP 1 180 799	2/2002		European				
	EP 0 030 856	6/1981		European				
	GB 1 414 228	11/1975		Great Britain				
	EP 0 694 977	1/1996		European				
	EP 1 237 193	9/2002		European				
	EP 0 878 804	11/1998		Encobeau				
	EP 0 801 427	10/1997		European				
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	EP 1 288 955	3/2003		European				
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	EP 0 920 059 A2	6/1999		European			
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	EP 0 869 511 A2	10/1998	1	European			
	EP 0 860 878 A2	8/1998	<u> </u>	European			
	EP 0 858 109 A2	8/1998		European			
	EP 0 844 671 B1	11/2002		European			
	EP 0 836 194 B1	5/2000		European			
	EP 0 788 165 A2	8/1997		European			
	EP 0 744 772 B1	8/2002		European			
	EP 0 739 097 A2	10/1996		European			
	EP 0 727 822 B1	8/1999		European		****	
	EP 0 727 820 A1	8/1996		European			
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	EP 0 725 402 B1	9/2002	<u> </u>	European					
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	EP 0 642 173 B1	7/1999		European			_		
	EP 0 606 758 B1	9/2000		European					
	EP 0 601 690 B1	4/2000		European					
	EP 0 599 506 A1	6/1994	ļ	European					
	EP 0 599 388 B1	8/2000	ļ	European					
	EP 0 579 566 A2	1/1994		European					
	EP 0 564 204 A2	10/1993		European					
	EP 0 537 677 81	8/1998	ļ <u>.</u>	European			_		
	EP 0 510 607 B1	2/1998		European					
	EP 0 465 961 B1	8/1995		European					
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Sheet 5 of 5 SERIAL NUMBER ATTY, DOCKET NO. PTO-1449 (Modified) 211.004-US 10/840,009 U.S. DEPARTMENT OF COMMERCE APPLICANT(S) PATENT AND TRADEMARK OFFICE Ferrant et al. GROUP ART UNIT FILING DATE INFORMATION DISCLOSURE STATEMENT 281B May 6, 2004 BY APPLICANT U.S. PATENT DOCUMENTS SUB FILING DOCUMENT DATE NAME EXAMINER CLASS CLASS DATE INITIALS NUMBER FOREIGN PATENT DOCUMENTS MOTALIZYANT DIÇESY St B EXAMINER DOCUMENT CLASS INITIALS NUMBER DATE COUNTRY EP 0 366 882 B1 5/1995 European 12/1994 European EP 0 359 551 B1 2/1990 European EP 0 354 348 A2 EP 0 350 057 B1 1/1990 European 7/1996 EP 0 333 426 B1 European EP 0 300 157 B1 5/1993 European EP 0 253 631 B1 4/1992 European 4/1997 EP 0 245 515 B1 European EP 0 207 619 B1 8/1991 European EP 0 202 515 B1 3/1991 European EP 0 175 378 B1 11/1991 European EP 1 191 596 A2 3/2002 European EP 1 233 454 A2 8/2002 European OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.) **EXAMINER** DATE CONSIDERED EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not

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Filed: May 6, 2004

APPLICANT: Ferrant et al.

TITLE: Semiconductor Memory Device and Method of Operating Same SERIAL NO.: 10/840,009

RECEIPT OF THE FOLLOWING PAPERS IS ACKNOWLEDGED

1. Fourth Information Disclosure Statement (1 page + Modified Form-PTO-1449 (5 pages) + References cited therein)

DATE: August 12, 2004

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